WHAT IS CLAIMED IS:

1. A driver circuit, comprising:

a first current path coupled to a first voltage;

a first switching circuit, under control of an input signal, to couple and uncouple said first current path to an output of the driver circuit;

a first current clamp, coupled in the first current path, to prevent a voltage at said output from reaching said first voltage; and

a first non-persistent charge boost circuit, coupled to the first switching circuit, to increase a rate at which said output switches toward said first voltage when said first current path is coupled to said output.

2. The driver circuit of claim 1, wherein the first current clamp comprises a resistor.

3. The driver circuit of claim 2, wherein the first non-persistent charge boost circuit comprises a capacitor, coupled in parallel with said resistor.

4. The driver circuit of claim 3, further comprising a delay circuit, coupled to the output of the driver circuit, wherein:

the first non-persistent charge boost circuit further comprises a field effect transistor that is coupled in parallel with said resistor via its source and drain terminals; and

the gate of the field effect transistor is coupled to an output of the

delay circuit.

5. The driver circuit of claim 3, further comprising:

a signal line coupled to said output; and

a receiver coupled to said signal line;

wherein said capacitor of the first non-persistent charge boost circuit has a value that is at least twice the sum of i) the capacitance of the signal line, and ii) the gate capacitance of the receiver.

6. The driver circuit of claim 1, further comprising a delay circuit, coupled to the output of the driver circuit, wherein:

the first non-persistent charge boost circuit comprises a field effect transistor that is coupled in said first current path via its source and drain terminals; and

the gate of the field effect transistor is coupled to an output of the delay circuit.

7. The driver circuit of claim 1, wherein the first switching circuit comprises a field effect transistor, the source and drain of which are coupled in said first current path, and the gate of which receives said input signal.

8. The driver circuit of claim 1, further comprising:

a signal line coupled to said output;

a receiver coupled to said signal line; and

a voltage clamp, coupled to said signal line in proximity to said receiver, to prevent a voltage at said receiver from reaching said first voltage.

9. The driver circuit of claim 1, further comprising:

a second current path coupled to a second voltage;

a second switching circuit, under control of said input signal, to couple and uncouple said second current path to said output;

a second current clamp, coupled in the second current path, to prevent a voltage at said output from reaching said second voltage; and

a second non-persistent charge boost circuit, coupled to the second switching circuit, to increase a rate at which said output switches toward said second voltage when said second current path is coupled to said output.

10. The driver circuit of claim 9, further comprising first and second delay circuits, coupled to the output of the driver circuit, wherein:

the first non-persistent charge boost circuit comprises a first field effect transistor that is coupled in the first current path via its source and drain terminals;

the gate of the first field effect transistor is coupled to an output of the first delay circuit;

the second non-persistent charge boost circuit comprises a second field effect transistor that is coupled in the second current path via its source

and drain terminals; and

the gate of the second field effect transistor is coupled to an output of the second delay circuit.

11. The driver circuit of claim 9, further comprising a delay circuit, coupled to the output of the driver circuit, wherein:

the first non-persistent charge boost circuit comprises a first field effect transistor that is coupled in the first current path via its source and drain terminals;

the second non-persistent charge boost circuit comprises a second field effect transistor that is coupled in the second current path via its source and drain terminals; and

the gates of the first and second field effect transistors are coupled to an output of the delay circuit.

12. The driver circuit of claim 9, further comprising:

a signal line coupled to said output;

a receiver coupled to said signal line; and

first and second voltage clamps, coupled to said signal line in proximity to said receiver, to prevent a voltage at said receiver from reaching either of said first or second voltages.

13. The driver circuit of claim 1, wherein the first current clamp is coupled

to the first non-persistent charge boost circuit to arm the first non-persistent charge boost circuit when the first current path is not coupled to said output.

14. A driver circuit, comprising:

a first current path coupled to a first voltage;

first switching means to couple and uncouple the first current path to an output of the driver circuit;

first current clamping means, coupled in the first current path, to prevent a voltage at said output from reaching said first voltage; and

first non-persistent charge boost means, coupled to the first switching means, to increase a rate at which said output switches toward said first voltage when said first current path is coupled to said output.

15. The driver circuit of claim 14, wherein said first current clamping means and first non-persistent charge boost means are coupled in parallel.

16. The driver circuit of claim 14, further comprising:

a second current path coupled to a second voltage;

second switching means to alternately couple and uncouple said second current path to said output;

second current clamping means, coupled in the second current path, to prevent a voltage at said output from reaching said second voltage; and

second non-persistent charge boost means, coupled to the second

switching means, to increase a rate at which said output switches toward said second voltage when said second current path is coupled to said output.

17. A method, comprising:

under control of an input signal, driving a signal line toward a first voltage by coupling a first current path to the signal line;

while the first current path is coupled to the signal line,

i) providing a non-persistent charge boost to the signal line, to increase a rate at which a voltage on the signal line switches toward said first voltage; and

ii) clamping current flow through the signal line to prevent said voltage on said signal line from reaching said first voltage.

18. The method of claim 17, further comprising clamping voltages at a receiving end of the signal line to a range of voltages that is smaller than a range of voltages allowed at a driven end of the signal line.

19. The method of claim 17, further comprising:

under control of said input signal, driving said signal line toward a second voltage by uncoupling the first current path from the signal line and coupling a second current path to the signal line;

while the second current path is coupled to the signal line,

i) providing a non-persistent charge boost to the signal line, to

increase a rate at which the voltage on the signal line switches toward said second voltage; and

ii) clamping current flow through the signal line to prevent a voltage on said signal line from reaching said second voltage.

20. The method of claim 19, further comprising clamping voltages at a receiving end of the signal line to a range of voltages that is smaller than a range of voltages allowed at a driven end of the signal line.

21. The method of claim 17, wherein, when the first current path is uncoupled from the signal line, the method used to clamp current provides a means to arm the charge boost.

22. The method of claim 17, wherein said current is clamped using a resistor.

23. The method of claim 22, wherein said non-persistent charge boost is provided by a capacitor, coupled in parallel with said resistor.

24. The method of claim 23, wherein said non-persistent charge boost is further provided by a field effect transistor, coupled in parallel with said resistor, and having a gate that is driven by a delayed version of the voltage on the signal line.